CHAPTER 1 : Numbering System

- If a data message is made up of 1s and 0s, it is **digital**. [Explanation: Digital is 1s and 0s, either binary or grey code]
- 0011011000101001 when transferred to computer language this information can be a representation of **hex, octal and decimal numbers**. [Explanation: Binary IS 'computer language' not a representation. Therefore, any answer with 'binary' in it is wrong.]
- A computer message 3B4 is **hexadecimal**.
- What systems uses base 10? **Decimal.**
- What systems use base 16? **Hexadecimal**.
- Binary coded decimal (BCD) format has a minimum of **four**.
- What is 1100001_2 - 101100_2? **110101 Base 2**.
- What is used for the power of 10? **Decimal**.
- In a computer, the address 3B8 is **hexadecimal**.
- What is a Grays converter? **Analogue to Digital.**
- 10101_2 + 11001_2 = **4610** [Explanation: 10101_2 + 11001_2 = 101110_2 = 4610]

SLIDE NOTES ***Numbering System***

DECIMAL SYSTEM

- Comprise of 10 digits from 0 to 9
- Base 10 system and indicate the power to base
- Example : 254_{10}
- POSITIONAL VALUE NUMBERING SYSTEM
- Example: 254_{10} consists of 2 HUNDREDS, 5 TENS and 4 ONE units.
  Written as: (2 X100) + (5 X 10) + (4 X 1) = (2 X 10^2) + (5 X 10^1) + (4 X 10^0)
- **Digit 2** carries the **MOST weight** and is known as **MOST SIGNIFICANT DIGIT (MSD)**
- **Digit 4** carries the **LEAST weight** and is known as **LEAST SIGNIFICANT DIGIT (LSD)**

BINARY SYSTEM

- Comprise of 2 digits (0 & 1) known as BITS
- Base 2 system. Example : 10112
- POSITIONAL value system 1011_2 = (1 x 2^3) + (0 x 2^2) + (1x2^1) + (1x2^0)
- **BINARY to DECIMAL Conversion**
  1011_2 = (1 x 2^3) + (0 x 2^2) + (1x2^1) + (1x2^0) = 8 + 0 + 2 + 1 = 1
- **DECIMAL to BINARY Conversion**
  - ✓ **SUCCESSIVE POWER OF 2.**
  - ✓ **SUCCESSIVE divide by 2** and record any remainder of division. [**FACTORISE**]
- Suitable for **SMALL** number
- **WORD**: Any number converted into BINARY form.
- **WORD LENGTH**: Each word is formed of a number of **BITS** (***BI***NARY DIG***ITS***)
- Example: 347_{10} = 101011011_2.
  WORD = 1010110112; Word length= 9 (because there is 9 bit)

OCTAL SYSTEM

- **OCTAL to BINARY conversion**
  Convert each OCTAL number into **3 bits BINARY** equivalent
- **BINARY to OCTAL conversion**
  Divide BINARY number into groups of 3 BITS starting from LSB
- If the FINAL group of MSB does **NOT have 3 BITS**, **ADD enough ZERO to make up 3 BITS**

Example : 635_8 TO BINARY. 6 3 5 110 011 101 Thus, $635_8 = 110011101_2$	Example :100111011_2 TO OCTAL. 100 111 011 4 7 3 Thus, $100111011_2 = 473_8$

HEXADECIMAL SYSTEM

- BASE 16.
- Composed of 16 digit Symbols 0 1 2 3 4 5 6 7 8 9 A B C D E F
- Example: 85D1B16
- **HEX to DECIMAL conversion**
  SUCCESSIVE POWER OF 16
- **DECIMAL to HEX Conversion**
  Divide with 16 and take the REMAINDER of division
- **HEX to BINARY Conversion**
  Convert each HEX digit into 4 bits BINARY equivalent.
- **BINARY to HEX Conversion**
  Divide BINARY number into groups of 4 bits STARTING at LSB.
- **HEX to OCTAL Conversion and vice versa**
  i) Convert HEX to BINARY
  ii)Convert BINARY to OCTAL
- **OCTAL to HEX Conversion and vice versa**
  i) Convert OCTAL to BINARY
  ii)Convert BINARY to HEX.

Example : $B2F_{16} = (11 \times 16^2) + (2 \times 16^1) + (15 \times 16^0)$ $= 2816 + 32 + 15$ $= 2863_{10}$	i.e. $B2F_{16}$ TO BINARY B 2 F 1011 0010 1111 THUS, $B2F_{16} = 101100101111_2$
Example : $3D_{16}$ convert to OCTAL i)Convert HEX to BINARY, 3 D 0011 1101 $3D_{16}=111101_2$ ii)Convert BINARY to OCTAL, 111 101 7 5 $111101_2=75_8$ Thus, $3D_{16}=75_8$	i.e. 110110101001_2 TO HEX 1101 1010 1001 13 10 9 D A 9 Thus, $110110101001_2=DA9_{16}$

OCTAL, HEXADECIMAL & BCD TABLE

Decimal	Octal	Binary
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	10	1000
9	11	1001
10	12	1010
11	13	1011
12	14	1100
13	15	1101
14	16	1110
15	17	1111

Decimal	Hexadecimal	Binary
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Decimal	Binary	BCD
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
6	0110	0110
7	0111	0111
8	1000	1000
9	1001	1001
10	1010	00010000
11	1011	00010001
12	1100	00010010
13	1101	00010011
14	1110	00010100
15	1111	00010101

BCD SYSTEM

- Binary Coded Decimal
- Number represented in 4 bits binary code
- Leaving a space between each group of 4 digits

a) Convert from decimal to BCD

i.	94	1001 0100
ii.	529	0101 0010 1001
iii.	2947	0010 1001 0100 0111

b) Convert from BCD to decimal

i.	011100001001	709_{10}
ii.	001101100100	364_{10}

ADDITION, SUBTRACTION & MULTIPLICATION

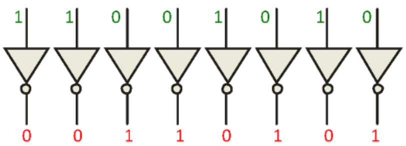
```
  0111
   00111        7
 + 10101       21
   -----      ---
   11100   =   28
```

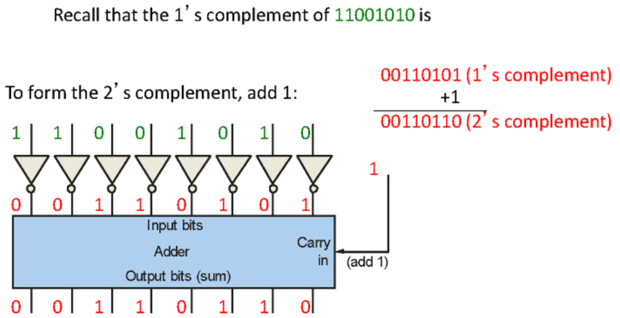
```
   111
   10101       21
   00111        7
   -----      ---
   01110   =   14
```

- Example : $1100_2 \times 11_2 = 100100$
- In computer, it is achieved by repeated addition.
- Ex: In decimal 2 x 4 is computed as 2+2+2+2 = 8

1'S & 2'S COMPLIMENT

- For example, the 1's complement of 11001010 is 00110101 (Using Inverters)
- The 2's complement of a binary number is found by adding 1 to the LSB of the 1's complement.





CHAPTER 2 : Logic Circuit

1. A NOR gate with both inputs inverted becomes a **AND gate**.
2. Adding invertors to the two inputs of an AND gate makes a **NOR gate**.
3. Which logic gate can be represented as a parallel circuit? **OR gate**.
4. Making an inverter from a NAND or NOR gate is achieved by **connecting the inputs**.
5. An AND gate output is 1 when inputs are **both 1**.
6. What sort of gate requires two positive voltages to operate? **AND**.
7. When will a NAND gate give logic 0 at the output? **When both inputs are at 1**.
8. The output of a NOT gate is logic 1. The input is **logic 0**.
9. When the voltage that represents a logic 1 state is less than the voltage that represents a logic 0 state, the logic being used is **negative**.
10. The output of an AND gate having two inputs A and B is logic 1. The two inputs will have the logic states of **A = 1, B = 1**.
11. The output of an OR gate having two inputs A and B is logic 0. The two inputs will have the logic states of **A = 0, B = 0**.
12. Which logic gate has both inputs high to get an output? **AND gate**.
13. A NAND and NOR to become a NOT gate have **inputs connected together**.
14. An AND gate with inverted inputs and an inverted output is equivalent to **an OR gate**.
15. Logic gates internal operating mechanisms are produced from **transistors**.
16. A logic 1 may be represented in an analogue system by (where Q is an output of a latch / flip-flop) **positive / magnetised / Q**.
17. What sort of gate requires two negative input voltages to operate? **NAND**.
18. In Positive Logic representation **state 1 is more positive than state 0**.
19. Switching within logic gates is normally achieved with the use of **diodes.**
20. The truth table of A =0011 B=0101 and =0110 indicates that the logic device is an **ECLUSIVE OR gate**.

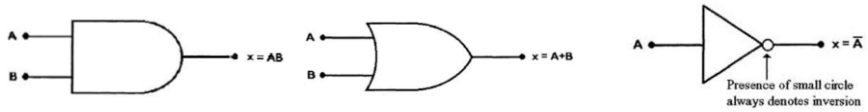
SLIDE NOTES ***Logic Circuit***

BOOLEAN CONSTANTS AND VARIABLES

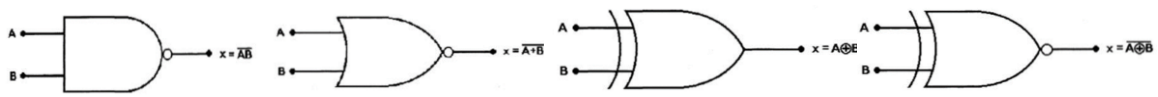
- Allowed 2 binary variables only : 1 & 0
- Represent voltages or logic level
- May represent (in circuit) : ON,CLOSED (logic 1) and OFF,OPEN (logic 0)
- Only 3 operation in Boolean algebra
- Logical addtion (+), Logical Multiplication (.) Logical Complimentation (-)

LOGIC SYMBOL WITH BOOLEAN EXPRESSION [Except Exclusive XOR & XNOR]

AND GATE OR GATE NOT GATE (**Know as Inverter**)



NAND GATE NOR GATE Exclusive OR (XOR) GATE XNOR GATE

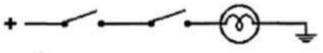


TRUTH TABLE

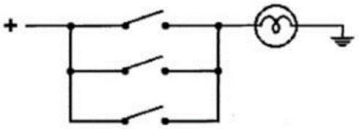
TYPE GATE		AND	NAND	OR	NOR	XOR	XNOR	NOT	
A	**B**	**X=AB**	**X=$\overline{AB}$**	**X=A+B**	**X=$\overline{A+B}$**	**X=A⊕B**	**X=$\overline{A\oplus B}$**	**A**	**X=$\overline{A}$**
0	0	0	1	0	1	0	1	0	1
0	1	0	1	1	0	1	0		
1	0	0	1	1	0	1	0	1	0
1	1	1	0	1	0	0	1		

SIMPLIFIED EQUIVALENT & GATE CIRCUIT

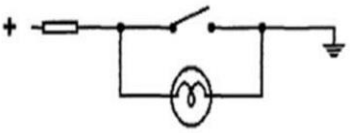
AND GATE



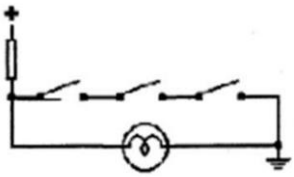
OR GATE



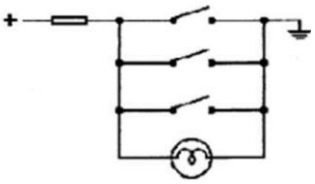
NOT GATE



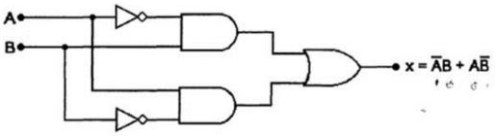
NAND GATE



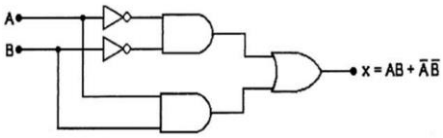
NOR GATE



XOR GATE



XNOR GATE



BOOLEAN EXPRESSION XOR & XNOR GATE

XOR GATE

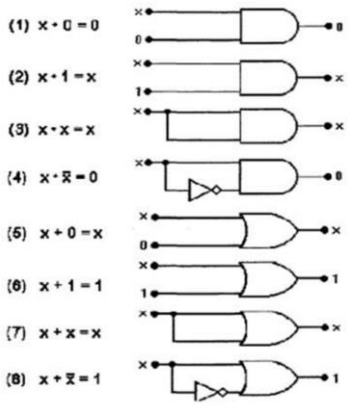
$$\bar{A}B + A\overline{B} = X$$

XNOR GATE

$$AB + \bar{A}\bar{B} = X$$

BOOLEAN THEOREM

- Single variable theorems



- Multivariable theorems

(9) $x + y = y + x$

(10) $x \cdot y = y \cdot x$

(11) $x + (y + z) = (x + y) + z = x + y + z$

(12) $x(yz) = (xy)z = xyz$

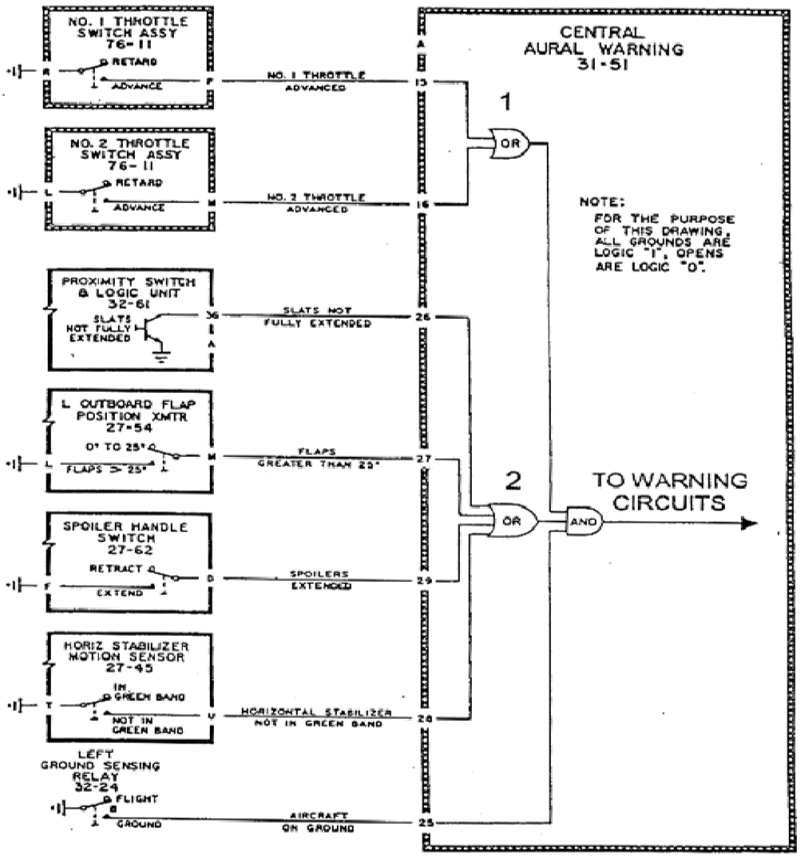
(13a) $x(y + z) = xy + xz$

(13b) $(w + x)(y + z) = wy + xy + wz + xz$

(14) $x + xy = x$

(15) $x + \bar{x}y = x + y$

APPLICATION



TAKE-OFF WARNING SYSTEM

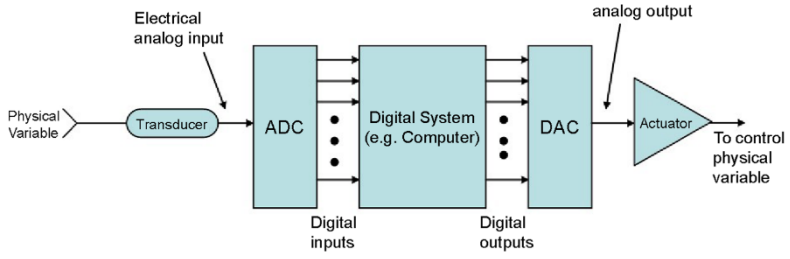
- Consist of 2 **OR gates** and an **AND gate**, with logic states received from **7 parameters**
- When either throttle leer is pushed forward, the switch at that position is made (advance) and there is a logic state 1 to OR gate1.
- 5 other parameters are sensed and logic states sent to OR gate2.
- If all the other parameters are in the take-off position, i.e.
  1. **Slats** not fully extended
  2. **Flaps** in take-off position i.e. less than 25°
  3. **Spoiler handle** in retract position
  4. **Horizontal stabilizer** in the green band (correct angle of incidence for take-off).Then the inputs to OR gate2 are all logic 0 and it's output to the AND gate is logic state 0.
- The aircraft on ground (weight switch) **gives another logic 1** to the AND gate, which has at this time 2 logic 1's and a logic 0
- If either of 4 inputs go out of take-off position eg flaps >25°,then the flap input signal to logic gate2 is logic 1 which makes the input to the AND gate logic 1
- The AND gate now has 3 logic 1's which now gives an output to warning circuits (CONFIG light and aural warning)

CHAPTER 4 : Data Conversion

1. If a signal has quantity in volts and physical position it is **Analogue**.
2. Within a computer controlled flight system, position feedback is converted from **analogue to digital.**
3. Physical variables in quantitative forms, such as voltage or angular rotation of a shaft are **analogue**.
4. A D to A converter would use a precision amplifier to **ensure that the output voltages remain accurate.**
5. A given transducer provides a voltage which corresponds to true heading. This voltage can be converted to 'bits' by using a **analogue to digital converter**.
6. An A to D converter uses successive approximation to **increase speed**.
7. An R-2R D to A converter uses **two values of resistors whose precision is not important**.
8. What does 1 represent in an analogue system? **Switches closed, magnetised**.
9. An analogue to digital converter where it counts up to binary state equal to the analogue input and then back down when this is reached is **a ramp type converter**.
10. Op amps generally used in ADCs and DACs are normally **high input impedance, low output impedance**.
11. Analogue logic 1 is **closed circuit, Logic Q=1**.
12. An ADC uses successive approximation to **increase speed**.
13. What is the quickest method of analogue to digital conversion? **Flash converter**.
14. An analogue to digital converter (ADC) requires the following; **a reference voltage, an input gate, a comparator**.
15. What is the Resolution of A/D and D/A converters? **Number of discrete values that can be represented by the digital word**.
16. Digital signals can be represented **by a series of integers**.
17. A Digital to Analogue Converter has a resolution of 0.3 Volts. What will be the analogue output when the digital input is 10110? **6.6 Volts DC**.
18. A number represented as a physical quantity, e.g. voltage or speed of rotation is **analogue**.

SLIDE NOTES ***Data Conversion***

Data Conversion- General



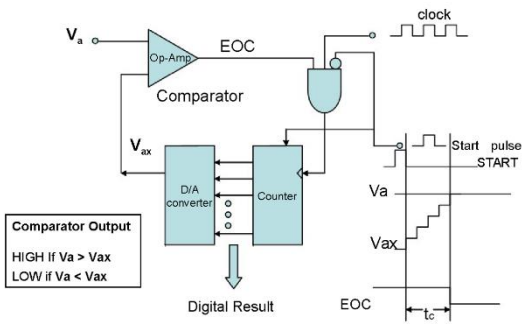
Analogue to Digital Converter (ADC)

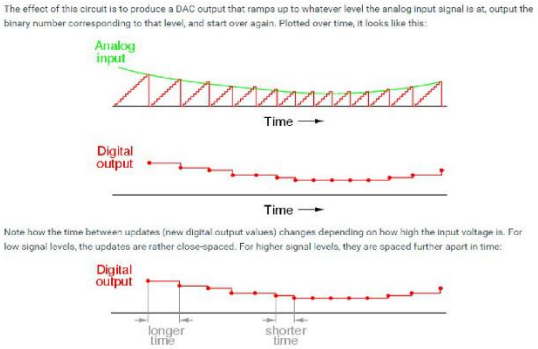
[Requires: Reference Voltage, Input Gate & comparator]

- Consists of:
  - ✓ Digital ramp converter (DRC)
  - ✓ Successive approximation ADC (SAC)
  - ✓ Integrated dual slope converter (IDSC)
  - ✓ The charge balancing converter (CBC)
  - ✓ Flash ADC (F.ADC)

	DRC	SAC	IDSC	CBC	F.ADC
Use	Counter	Register	Integrator	Differential Amplifier	
Advantages		Fixed Value Conversion Time, Faster than DRC	More accurate & high immunity noise		High Speed
Dis-advantages	Longer Conversion Time		Slower than SAC		More complex circuitry with increasing of the bits required, high cost and restricted
Application			Multimeter	Communication	

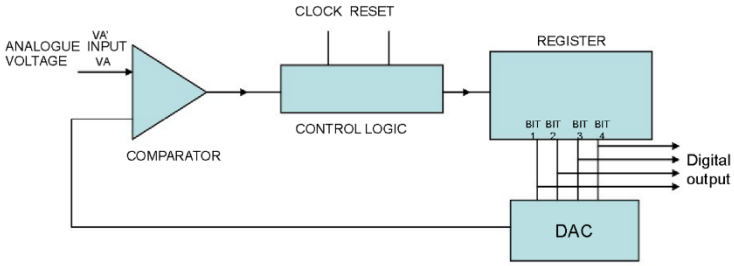
DIGITAL RAMP CONVERTER [Special component: Counter]





- The Ramp or Staircase type of Analog to Digital Converter **uses a counter** and a DAC (digital to Analog converter) to match the digital output to the analog input.
- It does this by converting the sequential count back into an analog signal and comparing the voltage level to the input signal. **Stopping the count** (Counter Function) when the two are equal. With this method of conversion, the output climbs from zero to the desired value and it is going to take longer to produce a correct output for higher voltages than for lower voltages.

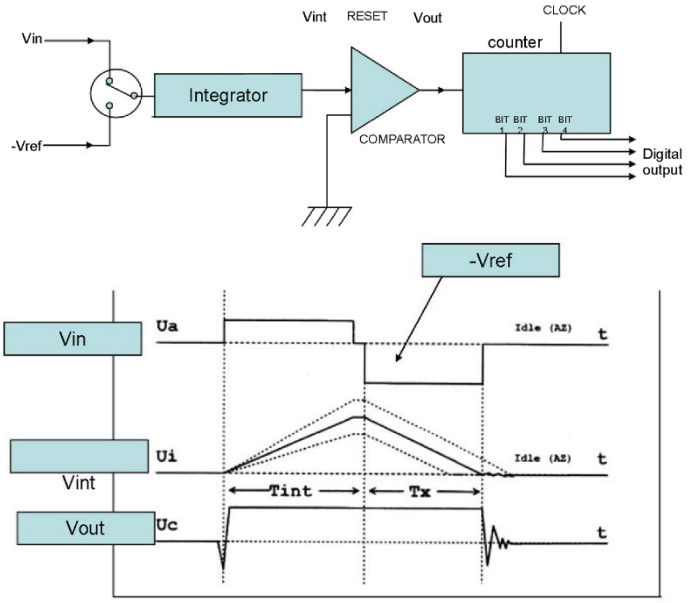
SUCCESSIVE APPROXIMATION ADC (SAC) [Special Comp: Register]



- Use **register** instead of counter (digital ramp) as input to DAC
- **Control logic** - modifies the content of the bit-by-bit until the output is equivalent of the VA
- Has **fixed value of conversion time** independent of the value of the analogue input therefore **faster than digital ramp**.

INTEGRATED DUAL SLOPE CONVERTER (IDSC)

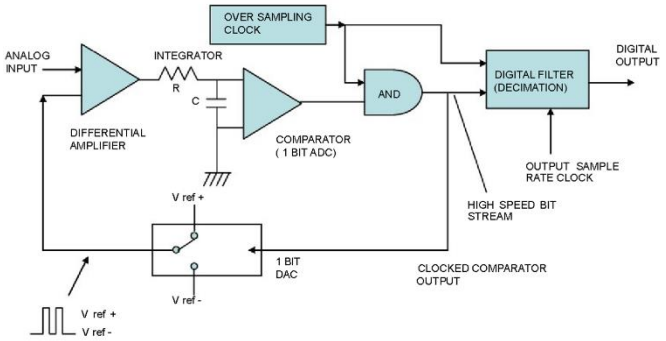
[Special Comp: Integrator]



- **Output from integrator** has two functions (input and time) to comparator
- Output of integrator slowly changing voltage,
  rising to peak - **ramp up (fixed time)** AND
  fall back to zero - **ramp down.**
  This time then is measured as **analogue input**
- Use **electronic switch** to change the integrator input voltage (Vin and Vref)
- **Slower than SAC** but **more accurate and high immunity noise**.
- Application: **multimeter** where accuracy is the prime concern than speed

CHARGE BALANCING CONVERTER (CBC)

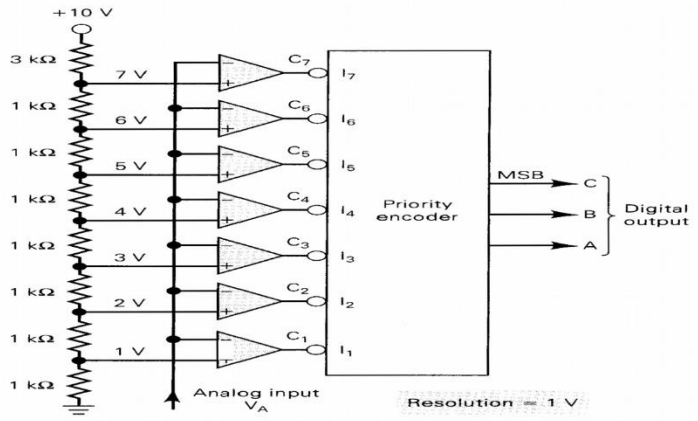
[Special Comp: Differential Amplifier]



- Use **over sampling technique** also known as **Sigma/Delta Modulation**
- Sampling analogue information more than sampling rate.
- **Differential amplifier**- produce error signal by comparing with analogue input
- The output from **differential amplifier** than is integrated then fed to comparator with output is clocked at over sampling rate.
- If integrator output is 0 than comparator output is 1 else 0. (comparator output is 1 bit ADC) • The term charge balancing used because the idea of converter is to maintain zero charge on the integrator capacitor

FLASH ADC (F.ADC)

[Special Comp: Integrator]

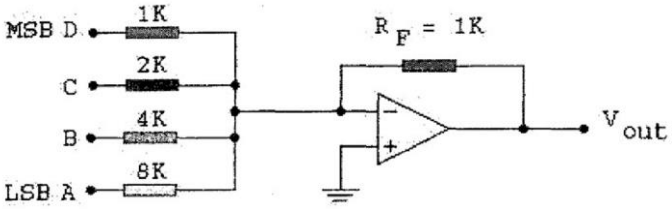


- This is **3-bit resolution** flash converter with **1V step size**
- The voltage divider sets up reference level for each **comparator-7 levels** corresponding to 1V.
- The analog input VA connected to the other input of each comparator.
- Outputs of comparators are **connected to active LOW priority encoder**.
- **VA <1V**, all comparator outputs C1 through C7 will be **HIGH**
- **VA>1V**, one or more comparator output will be **LOW**
- **Operate at high speed** due to no timing sequence, no clock signal, conversion as soon as VA is applied-only dependant on the propagation delay of the components
- n-bit converter **requires 2n** possible voltage level and 2n -1 comparators

Digital to Analogue Converter (DAC)

- Consists of:
  - ✓ OP-AMP Summing
  - ✓ R-2R Ladder DAC
  - ✓ Precision Level DAC
  - ✓ Current DAC

OP-AMP SUMMING



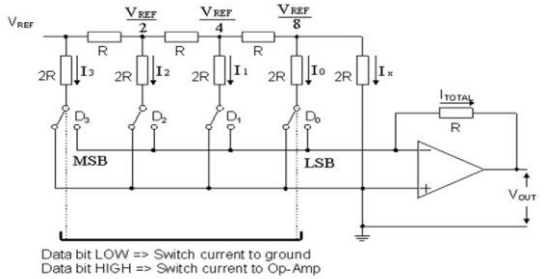
NOTE: The input resistor values are *BINARY WEIGHTED*

- The op-amp act as **summing amplifier**
- The output therefore Vo = RF x -(VD/RD+VC/RC+VB/RB+VA/RA)
- Example. If the input is 1001 and
  RF = 1kΩ and
  VD =VC=VB=VA= 5V
- Vo = 1k x (-(5V/1k) +0+0+(5V/8k)) = - 5.63V

Disadvantages

- Output voltages may not be ideal value due to
  - ✓ Variation in the input and feedback resistor
  - ✓ Logic level inputs not being exactly 0V or 5V
- Only suitable for small number of bit

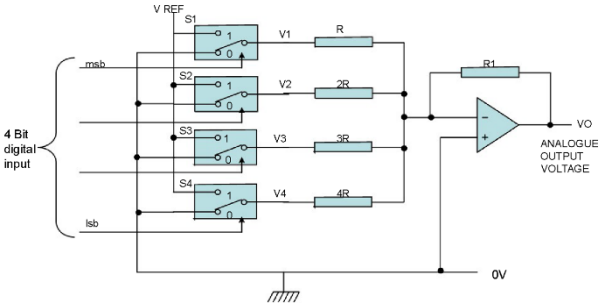
R-2R LADDER DAC



R-2R Digital to Analogue Converter (DAC)

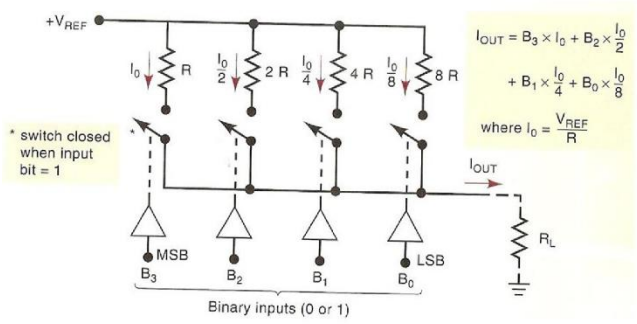
- Overcomes problems due to wide range of close value input resistor by using only 2 resistors
- But resistor has to be accurate
- Vout =-(Vref/2(N-1))x B
  B is the value of binary input
  N is the number of BITs

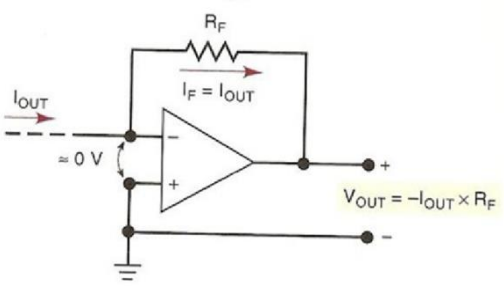
PRECISION LEVEL DAC



- To overcome the major disadvantage of the simple OP-AMP summing DAC
- Overcome using very precise resistor or by trimming
- The digital inputs cannot be taken directly from the output of FFs or logic gates due to the output logic levels of these devices are not precise values like 0V or 5V.
- Necessary to add circuitry between each digital input and its input resistor to the summing amplifier.
- Each digital input control a semiconductor switch
- When the input is HIGH, the switch closes and connects a VREF (precision reference supply) to the input resistor
- When LOW, the switch open
- VREF produces a very stable, precise voltage to generate an accurate analog output

CURRENT DAC





- Uses 4 current parallel path, each controlled by semiconductor switch
- The state of each switch is controlled by logic levels at the binary inputs(B0,B1,B2,B3)
- Current through each path is determined by an accurate reference voltage VREF and a precision resistor (binary weighted).
- The output current will be the sum of the individual current
- For IOUT to be accurate, RL should be a short to ground
- Accomplish by using an op-amp as a current-to- voltage converter.
- The op-amp negative feedback forces a current equal to IOUT to flow through RF to produce VOUT= -IOUT x RF
- VOUT will be an analog voltage that is proportional to the binary input to the DAC

CHAPTER 5: Basic Computer Structure

1. The advantage of DRAM over SRAM is has **a larger storage capacity per chip area**.
2. A BYTE is usually **an 8-bit word**.
3. What is the definition of baud rate? **1 bit per second.**
4. Which would have the least components? **ALU**.
5. What is EPROM? **Erasable programmable read only memory**.
6. How many bytes can be carried in a 32bit word? **4 bytes**. (Explanation. 8 bits per byte.)
7. Data is usually stored in **ROM**.
8. A basic computer would consist of **memory, input/output ports and CPU**.
9. DRAM **requires a refreshing charge**.
10. The CPU consists of **ALU, timing and control section, register**.
11. Where is the operating program for the CPU stored? **Memory unit**.
12. An EPROM **is non-volatile memory**.
13. A computer requires to operate, **a. data bus, a control bus, an address bus**.
14. What is the purpose of the ALU? **The part of the CPU unit where arithmetic and logic operations are carried out**.

SLIDE NOTES ***Basic Computer Structure***

COMPUTER TERMINOLOGY

- **BIT** - A binary digit (Binary digit)
- **BYTE** -Term for 8 bits word [1 byte = 8 bits]
- **BAUD RATE** – 1 bit per second
- **ADDRESS** -Numbers indicate the location of a word in computer memory
- **NIBBLE** - Word size of 4 bits (half byte) [Nibble = ½ byte = 4 bits]
- **WORD** -The number of bits that constitute a common unit of information as designated by the computer system.
- **SOFTWARE** - A program or instruction used to control a computer.
- **OPERAND** - Data that is operated on by computer as it executes an instruction.
- **OP CODE** - An instruction word that tell the computer what to do with OPERAND.
- **HARDWARE** - Components inside a computer.
- **FIRMWARE** - Program permanently recorded in computer hardware.
- **CPU (Central Processing Unit)** - Computer hardware that interprets and executes program instruction.
- **ACCUMULATORS** - Register that's collect the result of computation
- **IC** - Integrated circuit (combination of electronic components built onto a single substrate of semiconductor material. [Black Colour]

BASIC COMPUTER

- Consists of CPU, MEMORY, INTERFACE and INPUT/OUTPUT

CPU

- Consists of Register, ALU (Arithmetic Logic Unit) and Timing and Control Unit

REGISTER

- Consists of a number of storage location where a piece of data is kept OR,
- A special memory in microprocessor called STATUS REGISTER which normally made up of a single bit called FLAGS.

ALU (Arithmetic Logic Unit) [Least Components]

- Performs the arithmetic and logical operations.
- All calculation are performed in BINARY.

TIMING AND CONTROL UNIT

- Co-ordinates the internal operation of the microprocessor.
- Control the operation of ALU
- Generates instructions to execute/perform each program instruction.

MEMORY

- A device which stored data or information.
- Storage can be divided into 2 groups:
  a) MAIN MEMORY (INTERNAL)
    - ✓ Also, called WORKING MEMORY which in constant communication with the CPU.
    - ✓ FAST in operation.

  b) AUXILIARY MEMORY (EXTERNAL)
    - ✓ Also, called MASS STORAGE - Has huge storage capacity and NON-VOLATILE.
    - ✓ SLOWER than main memory.
- 2 types of memory which are ROM and RAM

INTERFACE

- Joining of dissimilar devices in a way to allow compatibility and coordination or synchronization of digital data between the computer and the input/output devices.
- Characteristic that should take into consideration:
  - Operation speed
  - Data format
  - Serial or parallel
  - Logic signal and etc

BUS SYSTEM

- Consists of 3 buses that carry all data and signal involved in computer's operation , which are; Address Bus, Data Bus and Control Bus.

ADDRESS BUS

- When CPU need to communicate with certain memory location of input/output device, it places an appropriate 16 bits address code on its 16 bits address output
- Address bus is unidirectional

DATA BUS

- Data bus is bidirectional with data to and from CPU
- During READ, the data bus acts as an input to the CPU.
- During WRITE, the data bus acts as an output from the CPU.

CONTROL BUS [Unidirectional and Bidirectional]

- The control bus synchronizes the activities of the microcomputer.
- RES: When LOW, causes the CPU to RESET at a particular start state.
- INT: Comes from input/output device, telling the computer that it wants to 'butt in' (interrupt). - R/W: Read don't write.

OPERATION OF BUS SYSTEM

- When it is desired to read the contents of a particular memory location:
  - ✓ CPU sends out the address of that location on the address bus and a 'memory read' control signal on the control bus.
  - ✓ The memory responds by outputting data stored in the addressed memory location onto the data bus.
  - ✓ 'Interrupt' from control bus tells the CPU that an external device needs to be read or serviced.

INSTRUCTION WORDS

- There are 2 main types of instruction Words:

  Single Address Instruction Word

  - Consist of an OP CODE and an OPERAND address.
  - Example: 4-bit OP CODE / 16 bit OPERAND ADDRESS

  Multi address Instruction Word

  - Consist of an OP CODE and more than 1 OPERAND address
  - A two address instruction word has an OP CODE and addresses for both OPERANDS needed to take part in the operation
  - Example: 2+3; ADD = OP CODE,
    2 = First OPERAND, 3 = Second OPERAND
  - If address include the result (3 address instruction word)
- Example of instructions for OPCODE
  - ✓ Arithmetic such as add and subtract
  - ✓ Logic instructions such as and, or, and not
  - ✓ Data instructions such as move, input, output, load, and store

MEMORY TERMS

- **MEMORY CELL** - A device or electrical circuit used to store a single bit
- **MEMORY WORD** - A group of bits in a memory that represents instructions or data
- **CAPACITY/DENSITY**- Specifies the number of bits that can be store in a computer memory
- **READ OPERATION**- The operation whereby the binary word stored at a specific memory address is sense and transferred to another device
- **WRITE OPERATION**- The operation whereby a new word is loaded into a particular memory address
- **ACCESS TIME** - A measure of memory devices operating speed
- **CYCLE TIME** - A measure of the entire time required to performed read and write operation.
- **NON-VOLATILE** – Keeps storing data when electrical power is removed.
- **VOLATILE** – Keep storing data when electrical power is keep.

TYPE OF MEMORY [ROM and RAM]

- **ROM - Read Only Memory**
  - PROM
  - EPROM
  - EEPROM
- **RAM - Random Access Memory**
  - STATIC RAM
  - DYNAMIC RAM

RAM

- Can write and read from RAM
- Temporary storage of program or data
- RAM address constantly changing as computer executes a program
- Volatile
- Often used as internal memory

STATIC RAM

- Can store data as long as power is supplied.
- They are flip-flop's that will stay in a given state.
- Available in BJT's or MOSFET
- BJT's are faster than MOSFET
- MOSFET's have greater capacity and used less power than BJT
- Required 6 transistor to store 1 bit data

DYNAMIC RAM [Larger Storage Capacity per chip area]

- Constructed using MOS technology.
- Required 1 transistor and 1 capacitor to store 1 bit data.
- Required Refresh logic for operation and required Refreshing Charge.

ROM

- Used to store data and information that are not change during the normal operation.
- Major used in storage of programs in microcomputers
- The process of entering data is called programming or burning in the ROM
- Non-volatile

PROM

- Programmable ROM
- Manufactured with fusible links used as electrical connection in the chip
- User programmable by burning the desired program.
- Once programmed, cannot be reprogrammed again.

EPROM

- Erasable Programmable ROM
- Can be reprogrammed as often as desired.
- Can be erased by exposing the EPROM to ultraviolet light through a window on the chip
- Erasure time is 15 to 30 minutes
- Erasing operation will erase the entire memory.

EEPROM

- Electrical Erasable PROM
- Ability to electrically erased and program individual words
- Erasing and programming are carried out by setting the polarities of a charge between the MOSFET gate and drain.

COMPUTER APPLICATION ON AIRCRAFT

- FMC (Flight Management Computer)
- EFIS (Electronic Flight Instrument System)
- EICAS (Engine Indication and Crew Alerting System)
- AUTOPILOT

CHAPTER 6: Data Buses

1. In arinc 629, LRUs are programmed to **transmit one transmits and one receives**
2. In aircraft use, fibre optic cables should comply with **ARIND 636 standard**.
3. ARINC 629 databus is **two cables, bi directional.**
4. An ARINC 573 data bus is used **to input into a Digital Flight Data Recorder**.
5. An ARINC 429 bus **uses a twisted shielded pair of wires**.
6. The ARINC 429 data bus word systems use **binary coded decimal**.
7. ARINC 573 is related to what system? **FDR**.
8. ARINC 629 databus is **one bus, bi-directional data flow**.
9. In an ARINC 429 wordstring, bits 1 to 8 represent **the monitored parameter**.
10. The parity bit in digital information is used **to check the validity of data information**.
11. ARINC 429 SDI word format is at bits **9-10** (SDI = Source Destination Ident.)
12. What is the parity bit for on an ARINC 429 bus?
    To check for corruption during transmission of a word.
13. An ARINC 429-word label format is **octal**.
14. How many LRUs can be connected to an ARINC 429 data bus? **20**.
15. An ARINC 429 bus uses **a twisted shielded pair of wires**.
16. ARINC 429 data bus systems uses **binary coded decimal**.
17. An ARINC 429 Binary Coded Decimal (BCD) word occupies word bits **11-29**.
18. An ARINC 429 system uses a **32-bit word over a twisted pair of wires**.
19. An ARINC 629 characteristic is **data can transmit in both directions down the data bus**.
20. What system uses base 8? **ARINC 429, in dataword labels only**.
21. The ARINC 429 low rate of transmission is **12-14 Kbits/second with high of 100 kBits/second**.
22. An ARINC 629 stub cable **connects bi-directional data between the LRU and current mode coupler**.
23. An aircraft databus system **can use both systems, ARINC 629 and ARINC 429 via system card files and signal gateways**.
24. ARINC 629 is used for **normal flight**.
25. How is the word label 206 written in ARINC 429? **Octal 01100001** (Explanation: Label is Octal - MSB to right - so yes, it is backwards.)
26. What is ARINC 561 used for? **Inertial Navigation Systems**.
27. An ARINC data word is bits 11-29, if bits 11-18 are patched which of the following would be the LSB bit? **19**.
28. Fibreoptic databus links are **bi-directional**.
29. A signal in an ARINC 629 system uses **a twisted pair of wires or fibre optics**.
30. One of the ARINC 429 formats is **BCD**.
31. The ARINC 429 system uses which of the following system to transfer data?
    Bi-directional return to zero.
32. Which of the following ARINCs is bidirectional? **629**.
33. ARINC 629 is transmitted using **fibre optics or twisted pair of wires**.
34. To create a bi-directional communications link within an ARINC 429 system **two databuses are required**.

35. In an Arinc 429 Word label-representing heading is 320, this is represented in bits 1- 8 as **00001011**.
36. What is the purpose of the parity bit on an ARINC 429 bus? **To indicate to the receiver that the data is valid**.

EXTRA NOTES

ARINC 429

- Bus **uses a twisted shielded pair of wires**.
- Data bus word systems use **binary coded decimal**
- In wordstring, bits 1 to 8 represent **the monitored parameter**.
- SDI word format is at bits **9-10** (SDI = Source Destination Ident.)
- Parity bit bus: **To check for corruption during transmission of a word**.
- Purpose Parity bit bus: **To indicate to the receiver that the data is valid**.
- Word label format is **octal**.
- **20 LRUs** can be connected to an ARINC 429 data bus.
- Bus uses **a twisted shielded pair of wires**
- Data bus systems uses **binary coded decimal**.
- Binary Coded Decimal (BCD) word occupies word bits **11-29**.
- Binary word occupies word bits **11-28**.
- System uses a **32-bit word over a twisted pair of wires**.
- Uses base 8, **in dataword labels only**.
- Low rate of transmission is **12-14 Kbits/second with high of 100 kBits/second**.
- An aircraft databus system **can use both systems, ARINC 629 and ARINC 429 via system card files and signal gateways.**
- **Octal 01100001**, the word 206 is written (Explanation: Label is Octal - MSB to right - so yes, it is backwards.)
- Word label-representing heading is 320, this is represented in bits 1- 8 as **00001011.**
- One of the formats is **BCD**
- Uses **Bi-directional return to zero** system to transfer data.
- **Two databuses are required** to create a bi-directional communications link within an ARINC 429 system.

SLIDE NOTES **ARINC429**

- Is a specification which define how avionic equipment and systems should communicate each other.
- Consist of pair of twisted wires with shielding.
- Point to point data bus and uses a unidirectional
  Data bus standard (Tx and Rx are on separate ports) known as the Mark 33 Digital Information Transfer System (DITS).
- Messages are transmitted at either 12.5 or 100 kbit/s to other system elements that are monitoring the bus messages
- Always transmitting either 32-bit data words or the NULL state

Electrical Characteristic

- Self-clocking and self-synchronizing system called 'bipolar return to zero'
- Transmitted in binary bit form, '1's and '0's are represent high voltage (+5v) and low voltage (-5v) level respectively for half of clock cycle then each pulse return.

Protocol

- Only one transmitter on a wire pair
- Always transmit 32-bit word or NULL state
- At least 1 receiver on wire pair and up to 20 receivers only
- Received depend on line length and the numbers of receivers connected to the bus.

Word Format

- **WORD** format is a 32 bit with five basic parts
  - LABEL
  - SOURCE /DESTINATION IDENTIFIER (SDI)
  - DATA FIELD
  - SIGN STATUS MATRIX(SSM)
  - PARITY BIT (P)
- **LABEL** - The first 8 bits of the word (octal coded). Identifies the information contained in the data e.g. airspeed, total air temp.
- **SOURCE/DESTINATION IDENTIFIER (SDI)** – used to identify the source/ destination of a word e. g. Which of a number of installations the word is coming from or needs to be directed into.
- **DATA FIELD** - contains specific data related to the LABEL. For binary word contained in bits 11- 28 and binary coded decimal (BCD) in bits 11- 29. Any bit not used are filled with logic 0's (pad bits)
- **SIGN STATUS MATRIX** - bits 29,30,31 for binary word and 30,31 for BCD. Identify characteristics of the word e.g. east/west, +ve/- ve and its status e.g. No computed data, failure warning, functional test or normal operation.
- **SSM code** for identity characteristic of the word for BCD data
- **SSM code** for status of word for BCD data
- **PARITY** - Uses odd parity e.g. Total number of logic '1' in the word must be an odd number. If not parity bit is set to 1. - Uses to check an error e.g. If receiving signal doesn't contain odd number 1, fault signal will be generated.

Transmission Order

- The least significant bit of each byte except the label is transmitted ahead of the data in each case. The order as follows: •8,7,6,5,4,3,2,1,9,10,11,12,13, 14,... .32.

EXTRA NOTES

ARINC 629

- Is an **Improvement of ARINC 429 system**
- LRUs are programmed to **transmit one transmits and one receives**
- Databus is **two cables, bi directional.**
- Databus is **one bus, bi-directional data flow .**
- Characteristic is **data can transmit in both directions down the data bus**.
- Stub cable **connects bi-directional data between the LRU and current mode coupler**.
- An aircraft databus system **can use both systems, ARINC 629 and ARINC 429 via system card files and signal gateways**.
- Used for **normal flight**
- A signal uses **a twisted pair of wires or fibre optics**
- Transmitted using **fibre optics or twisted pair of wires**
- ARINC 629 is **bidirectional**.

SLIDE NOTES **ARINC629**

- Additional ARINC standards are being developed.
- ARINC 629 is used on the new Boeing 777 Aircraft.
- It uses a high speed bi- directional bus capable of either periodic or aperiodic transmissions.
- Access to the bus is controlled by a sophisticated protocol involving wait periods, quiet periods and other rules.
- Data bus is unshielded, twisted pair of wires bonded and terminated at both ends.
- Data is send at rate 2 Mbps

ARINC 561

- Used for **Inertial Navigation Systems**.

ARINC 573

- Data bus is used **to input into a Digital Flight Data Recorder**
- Is related to **FDR system**.

ARIND 636

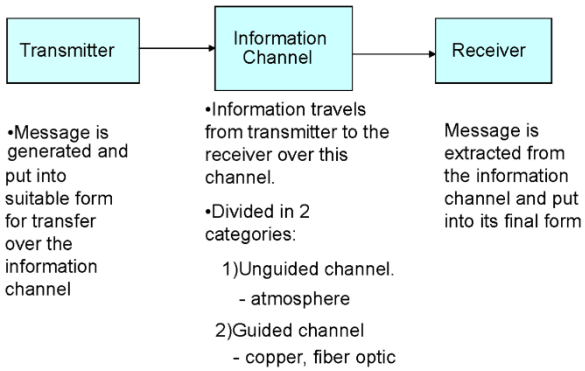
- In aircraft use, fibre optic cables should comply with **ARIND 636 standard.**

CHAPTER 7 : Fibre Optics

1. Some of the advantages of fibre optic cable over copper cables **are smaller in size and weight, non-conductive, higher security and higher bandwidth**.
2. A fibre optic cable consists of **a silica glass core with a cladding having a lower refractive index**.
3. Fibre optic cables **are immune to EMI**.
4. A disadvantage of a fibre optic cable is **end terminals are susceptible to environmental contamination**.
5. What kind of light is used in a fibre optic systems? **Infrared**.
6. A fibreoptic data bus used on an aircraft **can transmit on several channels at the same time**.
7. Light travels along a fibre optic by **reflection**.
8. What is the main disadvantage of a fibre optic data bus? **Expensive to install**.
9. Which of the following is an optoelectronic device? **Laser Diode**.
10. What is the advantage of a single mode fibreoptic over ordinary wire? **Large bandwidth**.
11. A fibreoptic light source is normally **a laser or LED**.
12. What maintenance problems are associated with fibreoptics? **Kinking and contamination of connectors**.
13. A fiberoptic cable to LRU connector should be connected **very carefully to ensure alignment and reduce light loss**.
14. What does a fibreoptic star connection do? **Provides direct point-to-point services to units on dedicated lines emanating from the central hub**.
15. Optical fibre losses are due to **absorption, scattering and reflection**.
16. Most fibreoptic connectors are designed so **the connectors cannot be over tightened**.
17. Light transmission in a fibreoptic cable is due to **repeated internal reflection**.
18. The name given to the joining of two fibreoptic cables by aligning them carefully and bringing them into close proximity of each other is **End to end**.
19. Fibreoptics relies on **light reflecting off cladding**.
20. Fibreoptic systems can transmit data in **both directions at the same time**.
21. For high bandwidth high-speed fibreoptic transmission what sort of cable would you use? **Single mode**.
22. What is the advantage of an ILD over an LED when used as a light source in fibre optics? **Lower frequency range**.
23. Speed of light in a fibreoptic fibre **is never greater then the speed of light in free space**.
24. What is the main cause of attenuation in fibreoptics? **Poor termination**.
25. What is the advantage of a laser diode over an LED? **Narrower bandwidth**.
26. A 'type A' fibre optic connector **would be used for connections not regularly disconnected**.

SLIDE NOTES ***FIBER OPTIC***

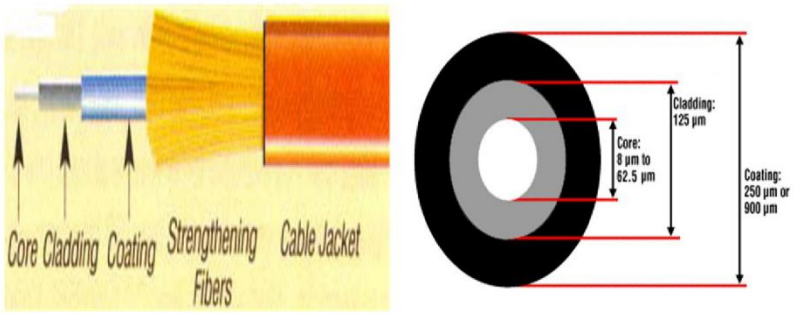
BASIC COMMUNICATION SYSTEM



FIBER OPTIC

- Fiber optics (optical fibers) are long, thin strands of very pure glass about the diameter of a human hair. They are arranged in bundles called optical cables
- Used to transmit high-speed transmission of data **using light** over long distances.
- Transmission depend on the optical property of **total internal reflection**.
- Maintenance Problem: **Kinking and contamination of connectors**.

STRUCTURE



- **Core** - Thin glass center of the fiber where the light travels
- **Cladding** - Outer optical material surrounding the core that reflects the light back into the core
- **Buffer coating** - Plastic coating that protects the fiber from damage and moisture
- Hundreds or thousands of these optical fibers are arranged in bundles in optical cables. The bundles are protected by the cable's outer covering, called a jacket.

TOTAL INTERNAL REFLECTION

- Core(n1) and cladding(n2) have different refraction index (n). n1(**Core**) is always **greater than** n2(**cladding**) [n1>n2]
- "When the angle of incidence exceeds a critical value, light cannot get out of the glass; instead, the light bounces back in."
- **Numerical aperture (NA)**
  - ✓ **Measure of maximum core angle** for light rays to be reflected down the fibre by total internal reflection
  - ✓ Snell's law: NA= $\sin\theta = \sqrt{(n1^2 - n2^2)}$
    n1 = refractive index of the core; n2 = refractive index of the cladding

TYPE

- Single-Mode
- Multi-Mode

SINGLE MODE

- **Small core diameter** (**5-10µm**) with an operating **wavelength** of around **1.5µm**
- Transmitter source: **laser diode**
- Only 1 incident angle,θ i.e. only 1 path and same velocity, eliminating distortion due to pulse lapping
- **Providing the least signal attenuation** and the **highest transmission speeds**, **large bandwidth** (typically 500 - 1500 MHz.km) and **longer distance**.
- Data is sent at **multi-frequency** (**WDM Wave-Division- Multiplexing**)

MULTI-MODE

- **Large core diameter** (**typically 100µm**) with operating **wavelength** around **1µm**.
- Support hundreds or thousands of light rays traveling at different velocities i.e. many angles of incident
- Transmitter source: **light emitting diode (LED)**
- Problem: **pulse broadening causing limitation on bandwidth**
- 2 type of multi-mode: **Step index** and **Graded Index**
- Easier to **launch optical power** and **facilitate the connecting of similar fibre.**
- **Total internal reflection** of light in a multi-mode optical fiber.

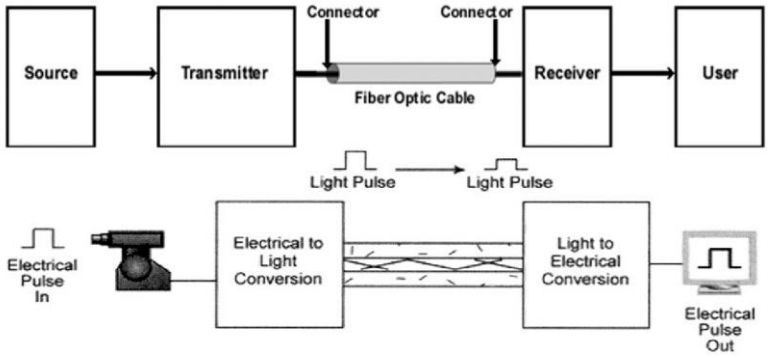
TERMINOLOGY

- **Attenuation**: signal loss within a fibre and measure in decibels per kilometer (dB/km)
- **Star coupler**: passive optical coupler which allows the light signals from each fibre stub to be coupled with other fibre stub and then into subsystems
- **Wavelength Division Multiplexing (WDM)**: signal of different wavelengths are sent down the fibre all together
- **Passive optical sensor**: optical sensor which do not require electrical supplies or any electronic processing. Used to monitor leading and trailing edge flap, spoilers, ailerons, rudder etc

OPTICAL SOURCES

- Laser Diode advantages over LED's:
  - ✓ They can be modulated at very high speeds.
  - ✓ They produce greater optical power.
  - ✓ They have higher coupling efficiency to the fiber optic cable.
  - ✓ Narrower bandwidth – Lower Noise Floor (Lower Frequency Range)
- LED's advantages over Laser Diode's:
  - ✓ higher reliability
  - ✓ better linearity
  - ✓ lower cost
  - ✓ Wide bandwidth – Increase Noise Floor (High Frequency Range)

TRANSMISSION OF FIBER OPTIC COMMUNICATION SYSTEM



- **Optical Source** - used to generate light signal. Can be either light-emitting diode (LED) or an injection-laser diode (ILD)
- **Transmitter** - Produces and encodes the light signals
- **Optical fiber** - Conducts the light signals over a distance. Light pulses move easily down the fiber- optic line because of a principle known as total internal reflection.
- **Optical regenerator** - May be necessary to boost the light signal (for long distances)
- **Optical receiver** - Receives and decodes the light signals. Can be either photodiode or phototransistor

ADVANTAGES OF FIBER OPTIC

- **SPEED**: Fiber optic networks operate at high speeds - up into the gigabits
- **BANDWIDTH**: large carrying capacity
- **DISTANCE**: Signals can be transmitted further without needing to be "refreshed" or strengthened.
- **RESISTANCE**: Greater resistance to electromagnetic, electrical isolation, low cross talk (interference)
- **MAINTENANCE**: Fiber optic cables costs much less to maintain
- **PHYSICAL**: Smaller size and weight than coaxial or copper cable buses.

DISADVANTAGES OF FIBER OPTIC

- Connectors have to be of high integrity
- No DC power transmission
- Minimum bend radii required
- Care when handling - no excessive pulling, pinching or crimping

MAINTENANCE OF FIBER OPTIC

- Repairing the cable by inserting an inline splice
  - ✓ 2 type of splicing : fusion and mechanical
  - ✓ **Cleaving** : The controlled breaking of a fiber so that its end surface is smooth
- Termination
- Testing

4 BASIC STEPS OF FUSION SPLICING

1. Stripping (Using Ethanol)
2. Cleaving
3. Fusion Process
4. Protection

7 STEPS OF TERMINATION

1. Connector (housing, body, dust cap and the strain relief boot)
2. Preparation
3. Stick in Fibre
4. Cleaving
5. Polishing
6. Visual Check
7. Testing

2 TYPES OF CONNECTORS

Type A

- used at production breaks i.e. **not regularly connected** and **disconnected**
- Multi-channel, **in-line (butt type)**
- Low loss

Type B

- Used to connect to LRUs, **frequent connected/disconnected**
- Multi-channel, **expanded beam (ball lens)**

TERMINOLOGY OF NETWORK

- **Bus network** - A network topology in which all of the terminals are attached to a transmission medium serving as a bus. All other terminals receive all signals transmitted from a terminal connected to the bus.
- **Bus** - Commonly called data bus. The term is used to describe the physical linkage between stations on a network sharing a common communication.

APPLICATION ON BOEING 777

- Avionics **Local Area Network (LAN)**
  - ✓ **AIMS** (Aircraft Information Management System)
  - ✓ **MAT** (Maintenance Access Terminal)
- **Cabin LAN** - Zone Network Controller - CFS (Cabin File Server)

TOPOLOGY

1. Bus Network
   - ✓ computer directly **connected on a main communication line**
   - ✓ Only 1 computer can communicate
   - ✓ Each computer communicates individually to the network
2. Star Network
3. Ring Network
   - ✓ Token - used to control access to the network